Liquid Architectures - The ρ-VEX Polymorphic VLIW Processor

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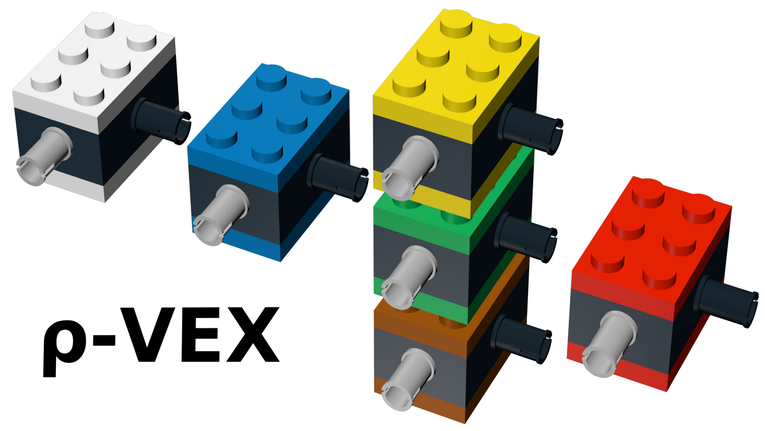
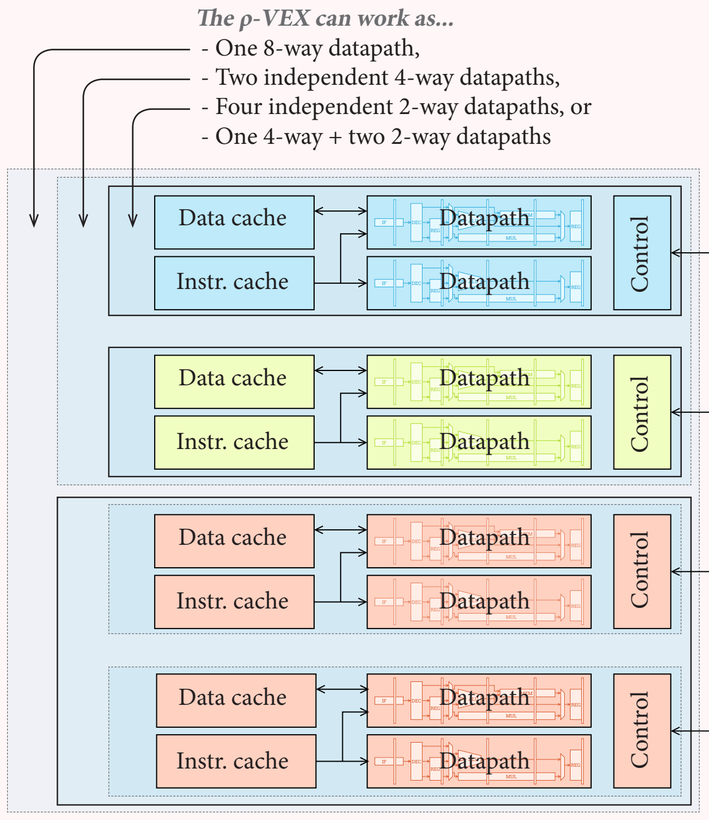


Overview

Observation - Modern embedded workloads are becoming **increasingly dynamic** (intensity, characteristics, criticality)
Problem - **Dynamic workloads** do not always map well to **fixed hardware**
Vision - A **dynamic computing platform** that continuously optimizes its hardware to all running tasks
Realization - **Dynamic assignment of caches and explicitly parallel datapaths** to different threads

The ρ-VEX can work as...
- One 8-way datapath,
- Two independent 4-way datapaths,
- Four independent 2-way datapaths, or
- One 4-way + two 2-way datapaths



ρ-VEX caches

The ρ-VEX data and instruction caches consist of **four cache blocks** each. These blocks can work together as sets, or completely independently. The caches remain **coherent and consistent** through reconfigurations; **no cache flushes are required**.

Runtime reconfiguration

ρ-VEX reconfiguration is **not FPGA reconfiguration**. It is all just control signals to multiplexers. Therefore, it only takes around **five cycles to reconfigure**, and the ρ-VEX is fully implementable using **ASIC technology**.

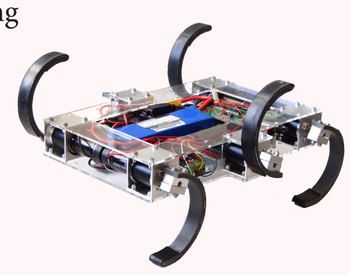
Hardware contexts

The default ρ-VEX configuration has **four hardware contexts**. When the processor is run-time-configured as four independent 2-way datapaths, each context stores the state for one of the datapaths. When not all contexts are active at one, the inactive contexts can store other program states for **fast context switching**. Each context can be assigned to every datapath/cache block for improved cache locality accross reconfigurations.

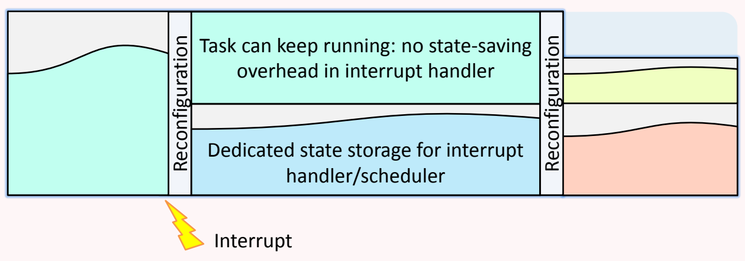
Application Examples

Robotics & Automotive

Typical requirements
- Low-latency event handling
- Image processing
- Mixed criticality

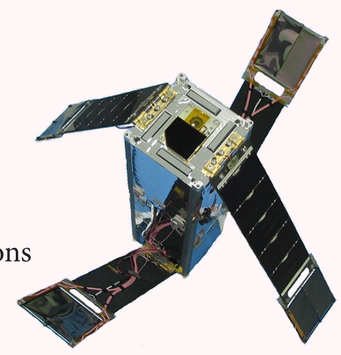


ρ-VEX advantages
- **Low interrupt latency**
- **Performance isolation**
- **Improved schedulability**
- Single architecture suitable for both DSP and general-purpose workloads **simplifies programming**

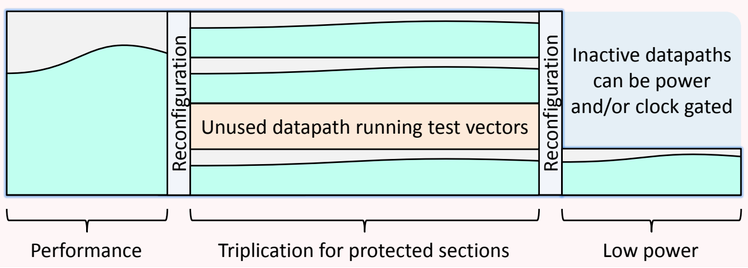


Space

Typical requirements
- High-radiation environment
- Low power consumption
- Signal processing



ρ-VEX advantages
- **Triplication** for critical sections
- Datapaths with permanent faults can be disabled
- **Low power** by gating datapaths



Education

Courses/labs

ET4078 - Modern Computer Architectures
ET4370 - Reconfigurable Computing Design

Four PhD. dissertations, two current candidates

Example topic:
- Runtime Adaptable VLIW Processors . . . . . Fakhar Anjam

Fifteen MSc. theses, five current students

Example topics:
- Streaming Caches . . . . . Koray Yanik
- FreeRTOS . . . . . Muneeb Yousaf
- Memory management . . . . . Jens Johansen

Two completed BSc. honours tracks, two in progress

Example topic:
- Floating Point . . . . . Matti Dreef

Six exchange students/staff members

Collaborations

European-Funded projects

2008 - 2013: ERA
- ST Microelectronics, Italy: . . . . . - Multi-core Simulator
  - Demonstrator development
- IBM Research Lab, Isreal: . . . . . - ρ-VEX GCC port
- Evidence, Italy: . . . . . - Exchange
  - Linux driver development

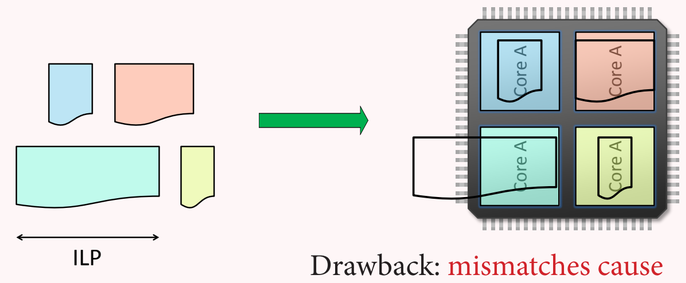
2014 - 2017: ALMARVI
- Philips Healthcare, Netherlands: . . - 2 Msc. projects
- Tampere University, Finland: . . . . . - Demonstrator development
  - Students exchanges
- CAMEA, Czech Republic: . . . . . - Demonstrator development

Other Universities
- Imperial College London, UK: . . . . . - Master's thesis topics
- Polytechnic Uni. of Turin, Italy: . . . - Fault tolerance
- Tallinn University, Estonia: . . . . . - Tool integration
- UFRGS, Brazil: . . . . . - Several exchanges
- University of Bristol, UK: . . . . . - Hardware integration

Computing Concepts

Traditional Platforms: Homogeneous Single-/Multicore

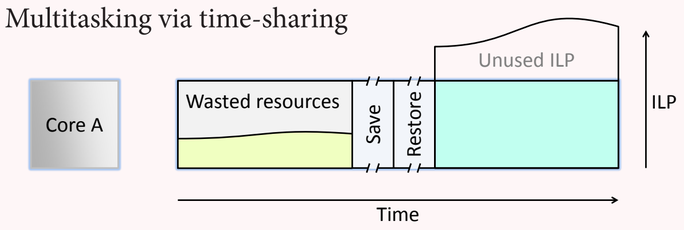
All programs map to the same core type



Drawback: mismatches cause reduced power efficiency!

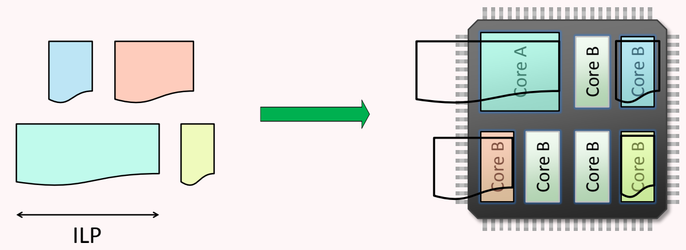
Single core:

Multitasking via time-sharing

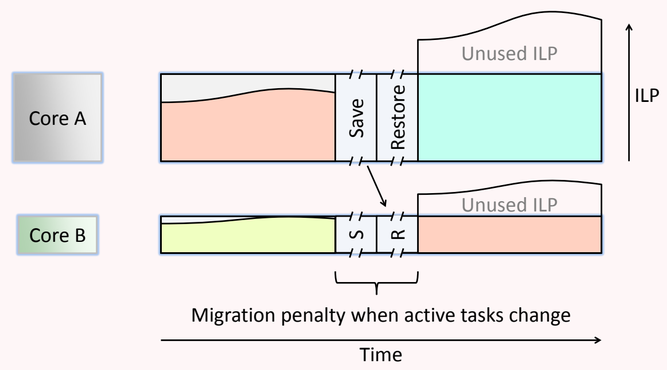


Current State of the Art: Heterogeneous Multicores

- Small and Large cores in a system
- Heavy programs on a large core: high performance
- Light programs on a small core: power savings

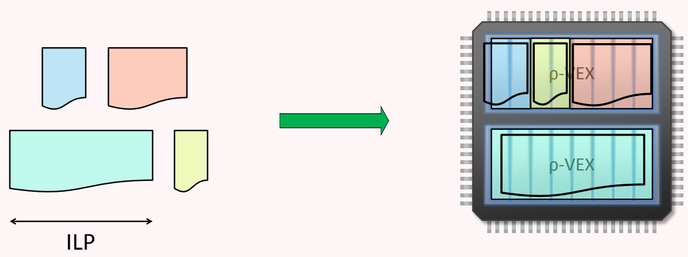


Drawbacks: Limited number core types
Still mismatches Migration penalty

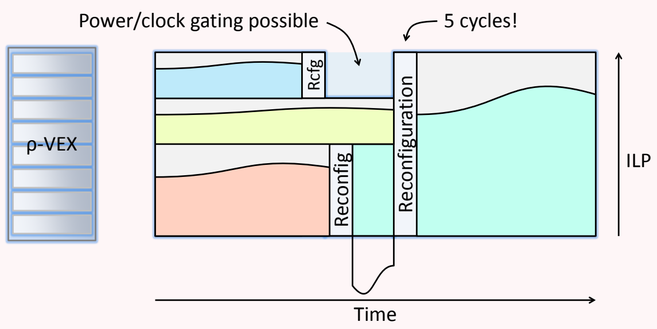


Our Approach: Dynamic Reconfiguration

- Large VLIW core can behave as multiple small cores
- Multiple contexts stored in hardware per core: used for fast context/configuration switching



Core can **adapt** to changes in the active task set **almost instantaneously**



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